

Amendments to the Specification:

Please replace paragraph [0062] with the following amended paragraph:

[0062] Referring now to Fig. 15, in another embodiment of the MRAM cell 60 for use in the memory cell array 52 of Fig. 11, a single junction MTJ device 1512 is connected in series with a single junction MTJ device 1514 attached to a resistor 1508. The resistor 1508 plays the role of sharing of bias voltage from a bit line 1128, 1130, 1132, and/or 1134. The resistor 1508 can be made from materials such as, for example, a layer of diamond-like carbon (DLC), a layer of Ti/Ta/X, where X is a metal, a layer of Ti/TaN/TiW, and other materials. The material and/or thickness of the resistive element are selected so that the resistive element does not behave as an anti-fuse ~~during~~ as discussed above with reference to Fig. 4.

Please delete the paragraph beginning at page number 25 which states:

MTJ 1504 = 0				
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Paragraphs [0065], [0066], [0067], [0068], and [0069] need to be renumbered as follows:

~~[0065]~~ [0063] The gate of each switching device 112 of the MRAM 60 can be attached to a word line 1120 and/or 1126 of the MRAM array 52. A multi-level reference circuit can read out the state of each bit, however the MRAM 60 can be limited by the chosen geometry and design rule for the integrated circuit

~~[0066]~~ [0064] The above embodiments illustrate only a few variations of the MRAM cell 60 structure. The present disclosure is not limited simply to structures with one switching device and two MTJ devices. Rather, it can be extended to allow for multiple MTJ devices attached to a single switching device.

~~[0067]~~ [0065] According to the above embodiments, the MTJ configurations 62 may not require active silicon-based isolation elements in order to isolate the memory cells in a memory array. The MTJ configuration 62 may be stacked memory elements or even three-dimensionally connected for fabrication on non-planar surfaces, curved, and spherical geometries, increasing device capacity. The MTJ configuration 62 may be fabricated by materials that are novel or non-conventional by semiconductor technologies.

[0068] [0066] An advantage of using MTJ configurations and configurations with multiple level sensing capabilities is that each MTJ configuration in the above discussed embodiments exhibits its own resistance characteristic due to the differing MR ratios of each MTJ configuration. The MR ratio of each MTJ can be controlled by differing the material or composition of each tunneling barrier 104 and 108. This allows each stacked MTJ configuration 62, as shown in Fig. 3, or the un-stacked configurations of Figs. 4 and 5 to simultaneously store two bits. The present embodiments of the MTJ configuration 62 have the ability to sense at least four different logical states based on the differing MR ratios, and this allows for a two times increase in memory density within the same or similar area used in a single MTJ configuration.

[0069] [0067] Based on the illustrated embodiments, one of ordinary skill in the art can easily apply the teachings of the present disclosure to create MTJ configurations that can store greater than two bits with greater than four levels of MR sensing. Likewise, one of ordinary skill in the art can easily apply the teachings of the present disclosure to other semiconductor devices and structures using multiple level sensing with different MR ratio MRAM cells.